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Design and verification of a thermoelectric energy harvester with stacked polysilicon thermocouples by CMOS process

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ABSTRACT

State-of-the-art CMOS semiconductor has been pushing below 32 nm process, and stacked system (also called chip stacking) will be the mainstream in IC foundry. Recent design of micro-thermoelectric generator (μTEG) is by using co-planar thermocouples to harvest ambient heat. A μTEG design based on stacked polysilicon thermocouples is developed in this work, in which the p- and n-thermolegs of a thermocouple are stacked and insulated. A thermal model is applied to analyze the optimal thermocouple size by matching their thermal resistance and electrical resistance. Analysis shows that the maximum power factor and voltage factor of an optimal thermocouple 100 μm × 4 μm × 0.275/0.18 μm (length × width × thickness for p-/n-thermolegs) is 0.0473 μW/cm^2 K^2 and 3.952 V/cm^2 K, respectively. The voltage factor is about 142% of that in co-planar design. Multiple thermocouples can thus be stacked for higher performance. Design verification by TSMC 0.35 μm 2P4M (2-poly and 4-metal layers) standard CMOS process shows that the stacked design with 120 μm × 4 μm × 0.275/0.18 μm thermocouples can achieve the power factor 0.0427 μW/cm^2 K^2 and voltage factor 3.417 V/cm^2 K.

1. Introduction

Increasing energy costs and upcoming environmental awareness are stimulating the development of energy harvesters to convert energy in ambient environment into usable electrical power. Among all kinds of energy harvesters, micro-thermoelectric generator (μTEG) converting waste heat is a promising candidate for on-chip power supply [1]. Conventional μTEG designs are often based on metals such as bismuth, tellurium and lead, while silicon-based design has the advantage of using present infrastructure in semiconductor industry. Standard CMOS process by thin-film deposition has been developed for very large scale integrated circuit. System-on-Chip (SoC) design integrating microsensor, RF transceiver, and power supply requires both monolithic CMOS circuit process while meeting the stringent space constraints.

Miniaturization of energy harvesters and integration with CMOS process have recently been addressed [2–4]. μTEG designs using polycrystalline silicon (poly-Si) and polycrystalline silicon germanium (poly-SiGe) thin films were recently developed [5–7]; however, their fabrication using wafer-bonding is low-yield. Better design is needed to facilitate cost-effective production. The μTEG design with co-planar p-/n-thermocouples has also been developed to harvest the heat flux from the top to the bottom surface [8,9], but the fabrication process remains incompatible to standard CMOS process. A most recent work of μTEG design in standard CMOS process has been reported [10]. Stacked system (also called chip stacking) is desirable CMOS semiconductor foundry beyond the state-of-the-art 45 nm process. Advanced design would naturally be based on the stacked system by having p- and n-polysilicon layer on top of each other so as to maximize area density and achieve better harvesting.

2. Stacked layer design

The effects of thermoelectric energy conversion are generally referred to Seebeck effect. Heavily doped semiconductors have been proposed to replace metals in thermocouple due to their much higher thermoelectric power. The generator performance is usually characterized by the figure-of-merit [11], which is proportional to operating temperature, electrical conductivity, and Seeback coefficient, but inversely proportional to thermal conductivity. As figure-of-merit becomes higher, the efficiency approaches the Carnot limit defined by the laws of thermodynamics. Improving energy conversion performance involves controlling the photon motion for heat and electrons for current; however, it is often difficult to increase the electrical conductivity without also increasing the thermal conductivity.

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Nomenclature

A	area
d	depth of thermal isolative cavity
I	electrical current
k	thermal conductivity
K	thermal resistance
L	length of thermocouple
N	number of thermocouple
P_o	specific power
Q	thermal flow
R	electrical resistance
S	Seebeck coefficient
t	thickness
T	temperature
U_o	open-circuit voltage
W	width of thermocouple
ϕ_p	power factor
ϕ_u	voltage factor

Subscripts

c	cold-side
g	thermocouple
h	hot-side
n	n-thermoleg
p	p-thermoleg
int	interface

A micro-thermoelectric generator shown in Fig. 1(a) has been proposed [10], across which the heat input from top surface is confined passing through in-plane thermolegs. Thermal isolation cavity design beneath the thermolegs is to eliminate heat leakage and facilitate better thermoelectric conversion. The design is based on co-planer thermocouples as illustrated in Fig. 1(b). The stacked design proposed in this work is shown in Fig. 1(c). A plurality of n-polysilicon on p-polysilicon thermoelectric layers overlies the silicon substrate to form a thermocouple in stack structure, where the two thermolegs are separated by an electrical insulation oxide layer. The stacked thermolegs are interconnected electrically to generate a voltage by the temperature difference between the cold and hot junctions. Similar to the co-planar design, a thermal insulation cavity is also formed beneath the thermocouples. Fig. 1(d) shows the top view and the cross sections of the stacked polysilicon thermocouples with the thermoleg length (L_g), width (W_g), thickness (t_p and t_n), to be used in analysis.

Fig. 2 illustrates the front-end process of the stacked design. The first thermoelectric layer has a line portion (p-thermoleg) on the dielectric layer and two protruding portions on another dielectric layer as shown in Fig. 2(a). The second thermoelectric layer (n-thermoleg) with the protruding portions on the dielectric layer is then deposited on the top to form a thermocouple, in which the line portion overlaps the first as shown in Fig. 2(b). Similarly the third and fourth layers are to form the second thermocouple as shown in Fig. 2(c) and (d), and the third thermocouple in Fig. 2(e) and (f). The two thermolegs of a thermocouple are separated by an insulation layer. Fig. 3 illustrates the back-end process of the metal layers to electrically connect the stacked thermolegs. The first metal layer in Fig. 3(a) and (b) connects the protruding portions of the thermcouples in series through the underlying conductive plugs. The second metal layer in Fig. 3(c) and (d) serves as the etching mask and electrically connects the first metal layer through the underlying conductive plugs. The third metal layer in Fig. 3(e) and (f) serves as the cold contact on the cold-end and electrically connects the second metal layer. The intermetal dielectric (IMD) layers can be etched by reactive ion etching (RIE) and the exposed substrate is isotropically etched by inductive coupled plasma (ICP) to form a cavity beneath the first dielectric layer to provide thermal insulation as shown in Fig. 3(g).

3. μTEG performance

A thermocouple as shown in Fig. 2 is composed of p-doped and n-doped-thermolegs with Seebeck coefficient S_p and S_n, respectively. In a generator with N thermocouples, the open-circuit output voltage is $U_o = NS\Delta T_g$, where $S = S_p - S_n$ is the combined Seebeck coefficient, and ΔT_g is the temperature difference, $\Delta T_g = T_h - T_c$, T_h and T_c is the hot- and cold-junction temperature. A thermal model is employed to simulate a generator with the hot-side, the thermocouple, and the cold-side with thermal resistance K_h, K_g, and K_c, respectively. Previous works have been plagued by undesirable Joule heating from relative large Ohmic resistance and by negligible temperature gradient across the thermolegs from small thermal resistance. Optimal design of the thermoleg geometry for higher output power, voltage, and current is thus necessary. The thermal and electrical resistances are determined by geometry of the thermolegs,

$$K_g = \frac{1}{N}\frac{L_g}{W_g}\left(\frac{1}{k_p t_p} + \frac{1}{k_n t_n}\right), \tag{1a}$$

$$K_h = \frac{1}{2N}\frac{t_h}{k_h A_h}, \tag{1b}$$

$$K_c = \frac{1}{2N}\frac{t_c}{k_c A_c} + K_{int}, \tag{1c}$$

$$R_g = N\frac{L_g}{W_g}\left(\frac{\rho_p}{t_p} + \frac{\rho_n}{t_n}\right). \tag{1d}$$

where L, W, t, A, K and k is the length, width, thickness, area, thermal resistance, and thermal conductivity, and the indices p, n, g, h, c, and int refer to p-thermoleg, n-thermoleg, thermocouple, hot-side, cold-side, and interface, respectively. Note K_c also includes the interface contact resistance. The μTEG performance is known strongly dependent on thermal resistance of interfaces during energy harvesting [12]. The precise estimation of K_{int} is difficult, and the metal-ceramic interface (1–20 cm^2 K/W) is assumed in the simulations and later validated experimentally at about 9 cm^2 K/W.

The power factor and voltage factor, $\phi_p = P_o/A\Delta T^2$ and $\phi_u = U_o/A\Delta T$, have commonly been employed to evaluate the generator performance. It has been shown that there will be little heat leakage by the 10 μm thermal isolation cavity design [10] and the power factor ϕ_p and voltage factor ϕ_u can be derived by using the thermal model [10,13]:

$$\phi_p = \frac{P_o}{A\Delta T^2} = \frac{R_g}{4A\Delta T^2 N^2 S^2} \left[\frac{1}{K_c} - \frac{1}{K_h} + 2C_2 \cos\left(\frac{1}{3}\arccos\left(\frac{C_1}{C_2^3}\right) + \frac{4\pi}{3}\right)\right]^2 \tag{2a}$$

and

$$\phi_u = \frac{U_o}{A\Delta T} = \frac{R_g}{A\Delta TNS} \left[\frac{1}{K_c} - \frac{1}{K_h} + 2C_2 \cos\left(\frac{1}{3}\arccos\left(\frac{C_1}{C_2^3}\right) + \frac{4\pi}{3}\right)\right]. \tag{2b}$$

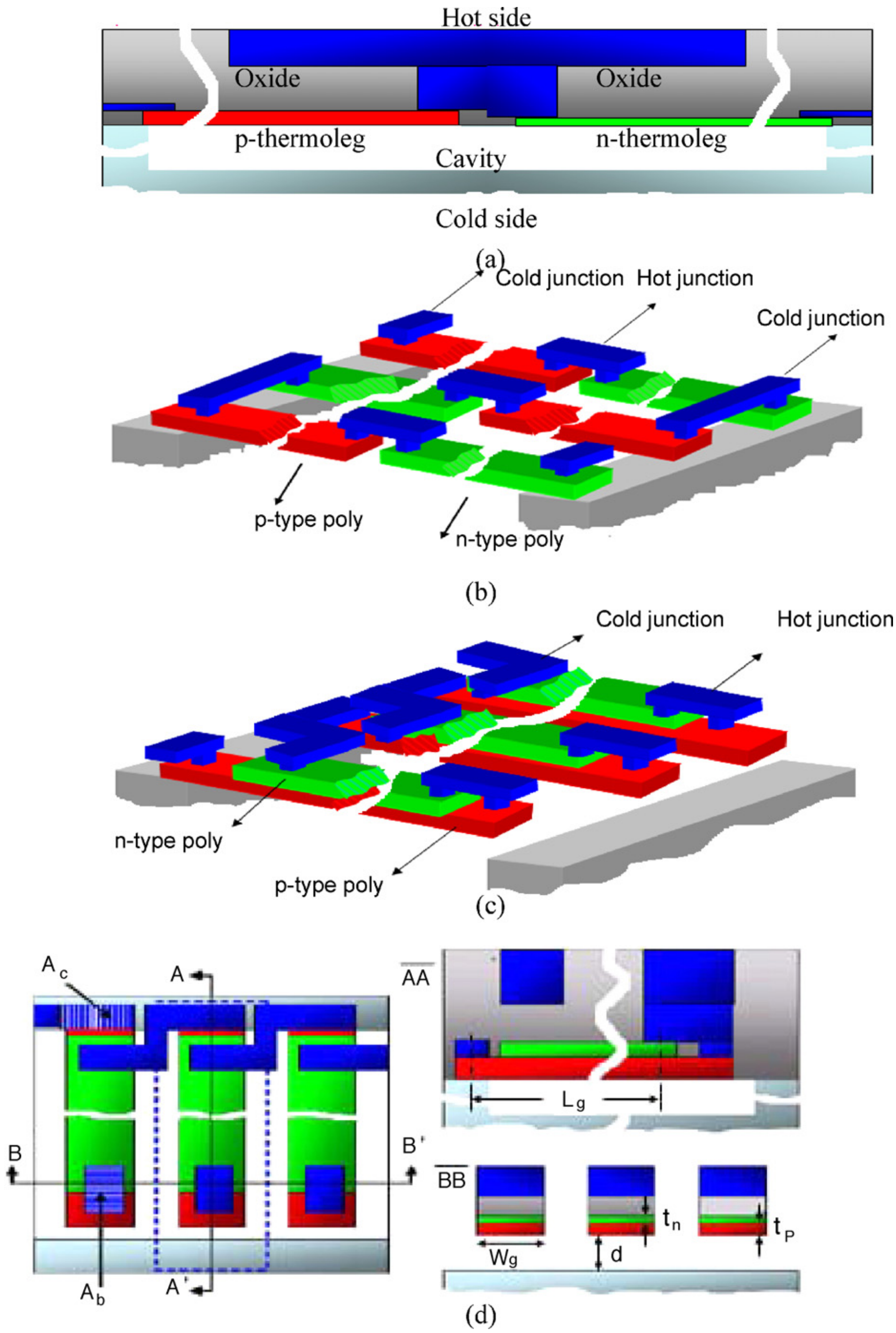


Fig. 1. (a) A μTEG with the conventional in-plane and cross-plane designs and a thermal isolation cavity to prevent heat loss, (b) the μTEG with the thermocouple of co-planar thermolegs, (c) the μTEG design proposed in this work with a stacked polysilicon thermocouple, and (d) the top view and the cross sections of the stacked polysilicon thermocouple indicating the design parameters.

where A is the total area of the μTEG, T_0 and T_1 are the cold-/hot-side temperature, and

$$C_1 = \left(\frac{1}{K_c} - \frac{1}{K_h}\right)\left(\frac{1}{K_c^2} + \frac{2}{K_c K_h} + \frac{1}{K_h^2} + \frac{4}{K_g K_h} + \frac{4}{K_g K_c}\right) + 2\frac{N^2 S^2}{R_g}\left(\frac{T_0}{K_c^2} - \frac{T_1 - T_0}{K_c K_h} - \frac{T_1}{K_h^2}\right) \quad (2c)$$

and

$$C_2 = \sqrt{\frac{1}{K_c^2} + \frac{2}{3K_c K_h} + \frac{1}{K_h^2} + \frac{8}{3K_g}\left(\frac{1}{K_c} + \frac{1}{K_h}\right) + \frac{4}{3}\frac{N^2 S^2}{R_g}\left(\frac{T_0}{K_c} + \frac{T_1}{K_h}\right)}. \quad (2d)$$

TSMC 0.35 μm CMOS process with two polysilicon layers and four metal layers (2P4M) commonly used in standard mixed-signal integrating digital, analog circuit and SoC is employed in analysis and design verification. Though the component geometry in IC design is different from that used in μTEG design, the data of thermoelectric material properties from standard CMOS process qualification are adopted in this work. The material properties of polysilicon in standard CMOS process are: S_p = 103 μV/K, S_n = −57 μV/K, ρ_p = 2.21 μOhm m, ρ_n = 0.813 μOhm m, k_p = 31.2 W/mK, k_n = 31.5 W/mK, the thermal conductivity of oxide on the hot-side (thickness 0.29 μm) k_i = 1.1 W/mK, and that of the Si substrate on the cold-side (thickness 650 μm) k_c = 168 W/mK. Consider symmetric design of equal length and width of the p- and n-thermolegs L_g = 1–150 μm,

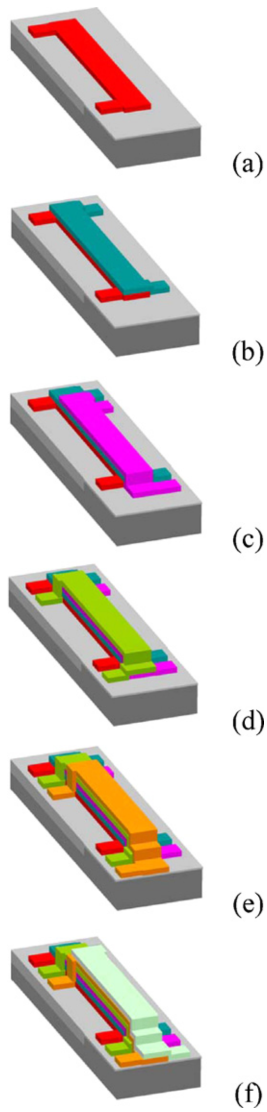


Fig. 2. The front-end process of thin-film depositions of a μTEG with three stacked polysilicon thermocouples: (a) the first p-thermoleg, (b) the first n-thermoleg, (c) the second p-thermoleg, (d) the second n-thermoleg, (e) the third p-thermoleg, and (f) the third n-thermoleg.

and $W_g = 4\,\mu$m, $t_p = 0.275\,\mu$m, $t_n = 0.180\,\mu$m, the oxide thickness $t_h = 0.29\,\mu$m on the hot-side and the substrate thickness $t_c = 650\,\mu$m on the cold-side. The dependence of the power and voltage factors of μTEG with one co-planar thermocouple [10], one stacked thermocouple, and two stacked thermocouples is shown in Fig. 4. The voltage improvement is also presented by stacking efficiency $\beta_u = U_o(N)/U_o(1)$ as listed in Table 1. P_o remains constant with the increase of N as shown in Fig. 4(a), because the increase of Ohmic R_g and the decrease of K_g cancel each other, but U_o increases significantly in the stacked design as shown in Fig. 4(b). This is desirable for efficient DC–DC conversion because the conversion efficiency is proportional to the input voltage [14]. For example, the application

Table 1
Comparison of stacked and co-planar μTEG design.

N # of thermocouple	L_g^* (μm)	ϕ_p (μW/cm^2 K^2)	ϕ_u (V/cm^2 K)	β_u (stacking efficiency)
1 (co-planar design)	71	0.0473	2.788	
1 (stacked design)	100	0.0473	3.952	142%
2 (stacked design)	143	0.0473	5.598	201%

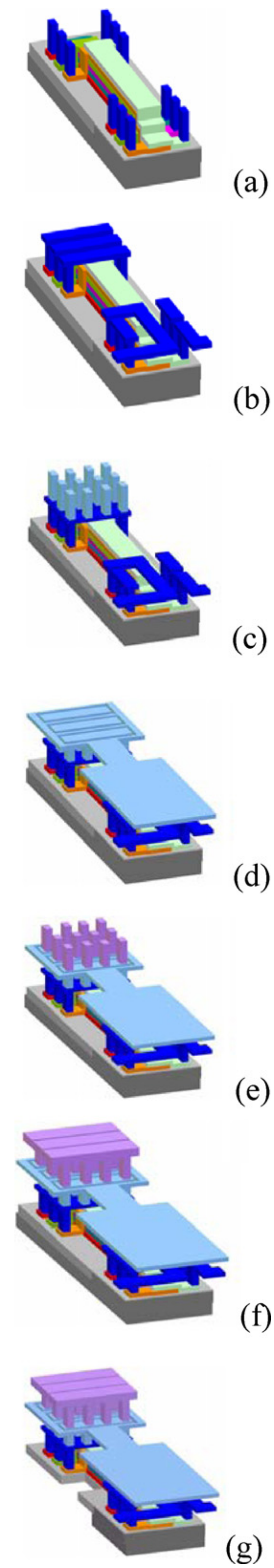


Fig. 3. The back-end process of the μTEG with stacked polysilicon thermocouples: (a) the first metal via, (b) the first metal interconnection, (c) the second metal via, (d) the second metal mask, (e) the third metal via, (f) the third metal end, and (g) the dry etching in creating the thermal isolation cavity.

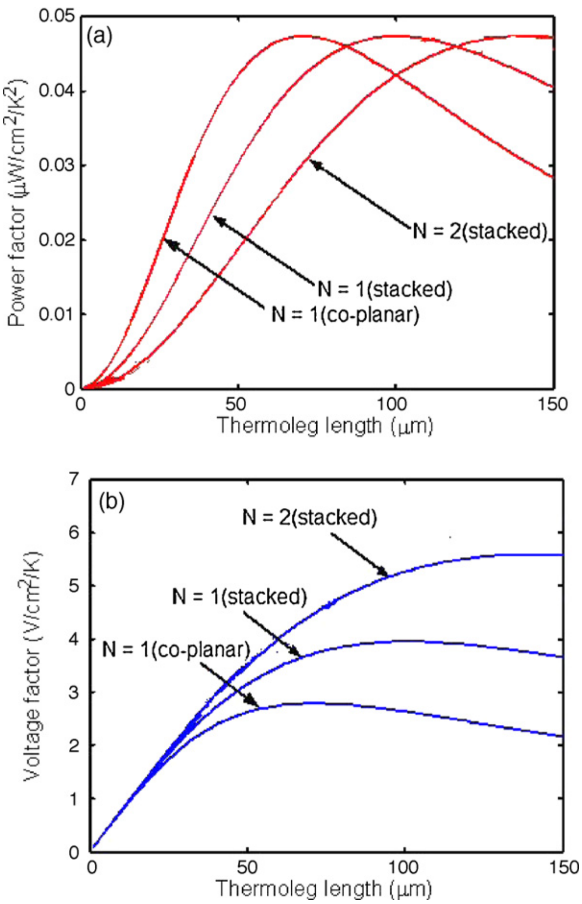


Fig. 4. (a) The power factor and (b) voltage factor of the μTEG ($W_g = 4\,\mu$m, $t_p = 0.275\,\mu$m, $t_n = 0.180\,\mu$m) in $N = 1$ (co-planar design) with p- and n-thermoleg on the same plane, $N = 1$ (stacked) design of a thermocouple with the n-thermoleg on top of the p-thermoleg, and $N = 2$ (stacked) design of two thermocouples.

circuit can have 42% more of converted power from the stacked polysilicon thermocouple than the co-planar, or more than 100% improvement from the two stacked thermocouples. μTEG design with higher number of stacked thermocouples is desirable in reducing the cost in deposition, photolithography, and etching, as the mask tooling of photolithography accounts for major expense. Note that the design using more stacks requires longer L_g, leading to higher K_g for thermal resistance matching in the thermocouples.

4. Stacked design by CMOS process

TSMC 0.35 μm 2P4M standard CMOS process is employed in this work and the cross section is shown in Fig. 5(a) with polysilicon (POLY1–2), aluminum (M1–4), intermetal oxide (IMD1–4), gate oxide (GOX), field oxide (FOX), capacitor oxide (COX), metal contact (CO), and metal via (VIA1–3) layers on a single crystallized silicon substrate. The patterned polysilicon layers serves as the thermolegs: POLY1 layer as the p-thermolegs and POLY2 layer as n-thermolegs as illustrated in Fig. 2(c), and they are interconnected by the aluminum pads to form the hot/cold junctions on the oxide layer. The top aluminum layer serves as the mask in post-process to protect the thermocouple when etching the thermal isolation cavity. The GOX layer serves as electrical isolation at the cold junction to prevent short circuit, and FOX as the thermoleg protection during isotropic silicon etching. M1 layer serves as the interconnections of thermolegs. M2, M3, and M4 layers as thermal conductors at the hot junctions, and M3 and M4 layers also as the etching masks during post-process, and CO and VIA1-3 as the interconnections

Table 2
Measured power and voltage factors of the μTEGs.

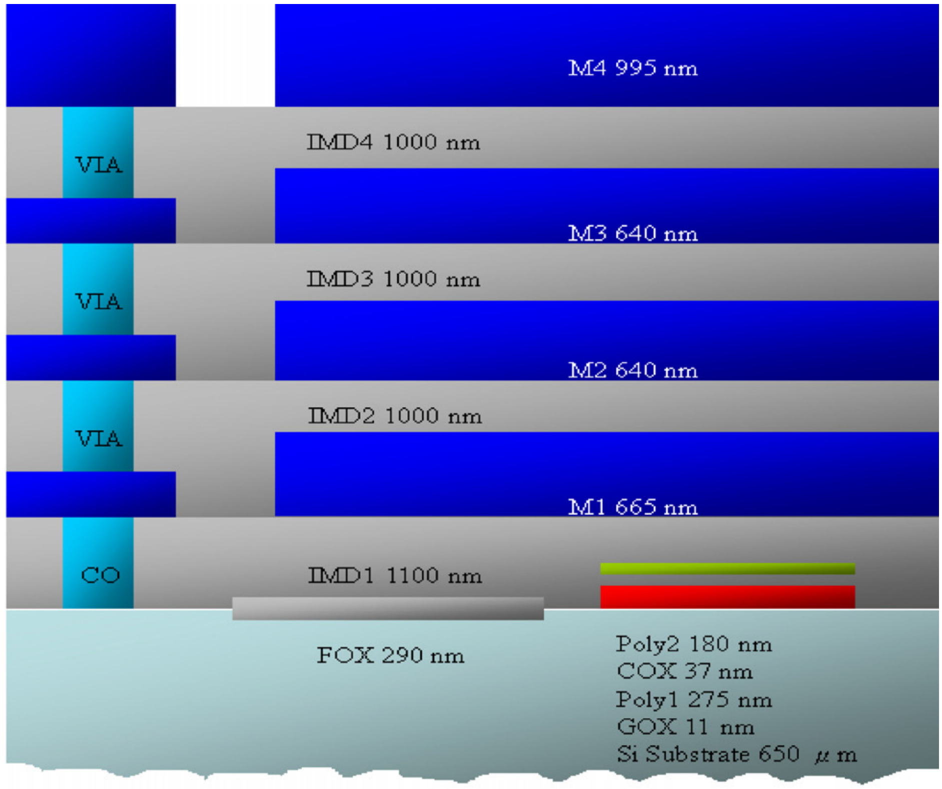
No.	$L_g \times W_g$ (μm)	U_o (mV)	I (μA)	ϕ_p (μW/cm² K²)	ϕ_u (μW/cm² K²)
#1	20 × 4	2.0	0.1	0.0021	0.833
#2	30 × 4	3.9	0.2	0.0081	1.625
#3	40 × 4	5.6	0.3	0.0175	2.333
#4	60 × 4	7.2	0.4	0.0300	3.000
#5	120 × 4	8.2	0.5	0.0427	3.417
#6	20 × 8	2.1	0.2	0.0044	0.875
#7	30 × 8	2.9	0.3	0.0091	1.208
#8	40 × 8	3.8	0.4	0.0158	1.583
#9	60 × 8	5.2	0.6	0.0325	2.167
#10	120 × 8	5.5	0.7	0.0401	2.292

of the layers. Fig. 5(b) shows a portion of the 2000 μm × 2000 μm chip with different thermoleg width and length as listed in Table 2. Test structures are located around the perimeter for measuring the thermoelectric properties, and each test structure is a cantilever imbedded with different thermoelectric material from the fixed- to the free-end. Pads for electrical connection are fabricated by patterning the top metal layer M4 into squares of 100 μm × 100 μm with 10 μm trenches around, and M3 serves as the etching protection for the structure beneath.

The 10 μm thermal isolation cavity has been implemented to maintain the temperature difference between the hot and cold junctions and to prevent heat leakage via the substrate. The etching window of the cavity is 4 μm in width, dictated by ICP for higher thermocouple density. The width of thermocouples is selected at 4 μm or 8 μm to ensure low contact resistance and complete etching. The stacked thermolegs are deposited and patterned by CMOS process as shown in Fig. 6(a), followed by the post-process of vertical SiO_2 etching with the top aluminum layers as the etching masks to form the slit surrounding the thermolegs in Fig. 6(b), and similarly the isotropic Si etching to form the cavity beneath the thermolegs for thermal isolation in Fig. 6(c). SiO_2 etching is by ICP using C_4F_8 and incorporating O_2 for polymer formation on the etching sidewalls as the protection. Isotropic Si etching is RIE using SF_6 for desired etching rate of 1 μm/min in vertical and 0.5 μm/min in lateral direction. Note in Fig. 6(c) that the stacked thermolegs are insulated by oxide layer. Fig. 6(d) shows the μTEG with stacked polysilicon thermocouple of 20 μm × 8 μm.

The μTEG performance is characterized by 20 K temperature difference from a heating wire and commercial cold plate (thermoelectric cooler). The μTEG chips are attached to a cold plate by thermal conductive gel, while a resistive hot wire is applied on the top surface of the chip. K_{int} in Eq. (1c) is validated experimentally by curve fitting the simulation results from the thermal circuit model, and the result at about 9 cm² K/W falls within the metal–ceramic interface of 1–20 cm² K/W. The output power and voltage is measured via the metal pads with the probe station (Wentworth Lab, 0-035-0923) and the multimeter. The measured data are shown in Table 2, in which the set of 120 μm × 4 μm has the highest power factor 0.0427 μW/cm² K² and the largest voltage factor 3.417 V/cm² K, and they are compared with the μTEGs reported in the literature in Table 3. The first thin-film μTEG was developed by Glosch et al. [15] in which the thermocouples are doped silicon and aluminum, each of 7 μm wide and 500 μm long, to generate 1.5 μW at 10 K temperature difference, or power factor of 0.0091 μW/cm² K². Though having higher power factor, the membrane configuration with parallel thermal flow is impractical for on-chip thermal harvesting and it is not CMOS compatible. The recent designs using poly-SiGe with a measured power factor 0.0051 μW/cm² K² [5], another using polysilicon μTEG with 0.00137 μW/cm² K² [7], and a recent polysilicon μTEG with 0.00363 μW/cm² K² [9] are an order smaller than

(a)



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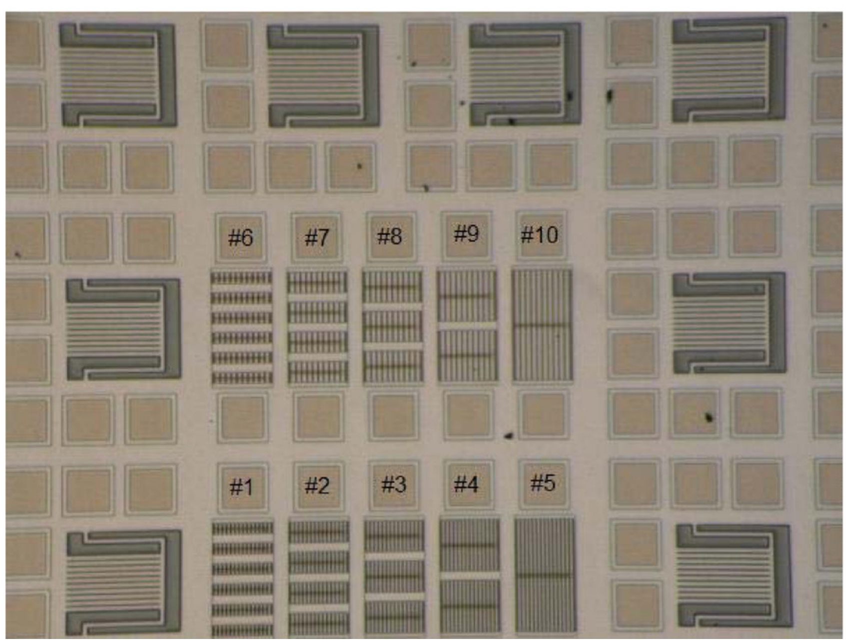

Fig. 5. (a) The cross section of TSMC 0.35 μm 2P4M foundry process and (b) the photo of a portion of the 2000 μm× 2000 μm chip with the μTEGs (#1–10 in Table 2) in the center and test structures in validating the thermoelectric properties in the perimeter.

this work. Their fabrication using wafer-bonding is also low-yield and may be unsuitable for batch manufacturing. A CMOS generator using polycrystalline silicon (poly-Si) and polycrystalline silicon germanium (poly-SiGe) thin films as developed by Strasser et al. [13], in which the thermolegs of 6 μm width and 18.5 μm length delivers a power factor of 0.00426 $\mu W/cm^2 K^2$. Though the power factor is about the same in this work, but the additional etching process requires modified CMOS process and thus may jeopardize the process stability [10]. A μTEG based on co-planar thermocouple design has improved the power factor to 0.0417 and voltage factor to 2.417. Fig. 7(a) and (b) shows the simulation of power factor for L_g = 1–150 μm, W_g = 4 μm and 8 μm. The proposed μTEG is shown to have optimal dimension in delivering the power factor of 0.0427 $\mu W/cm^2 K^2$ and voltage factor of 3.417 $V/cm^2 K$. The fabrication process is CMOS compatible suitable for engineering implementation.

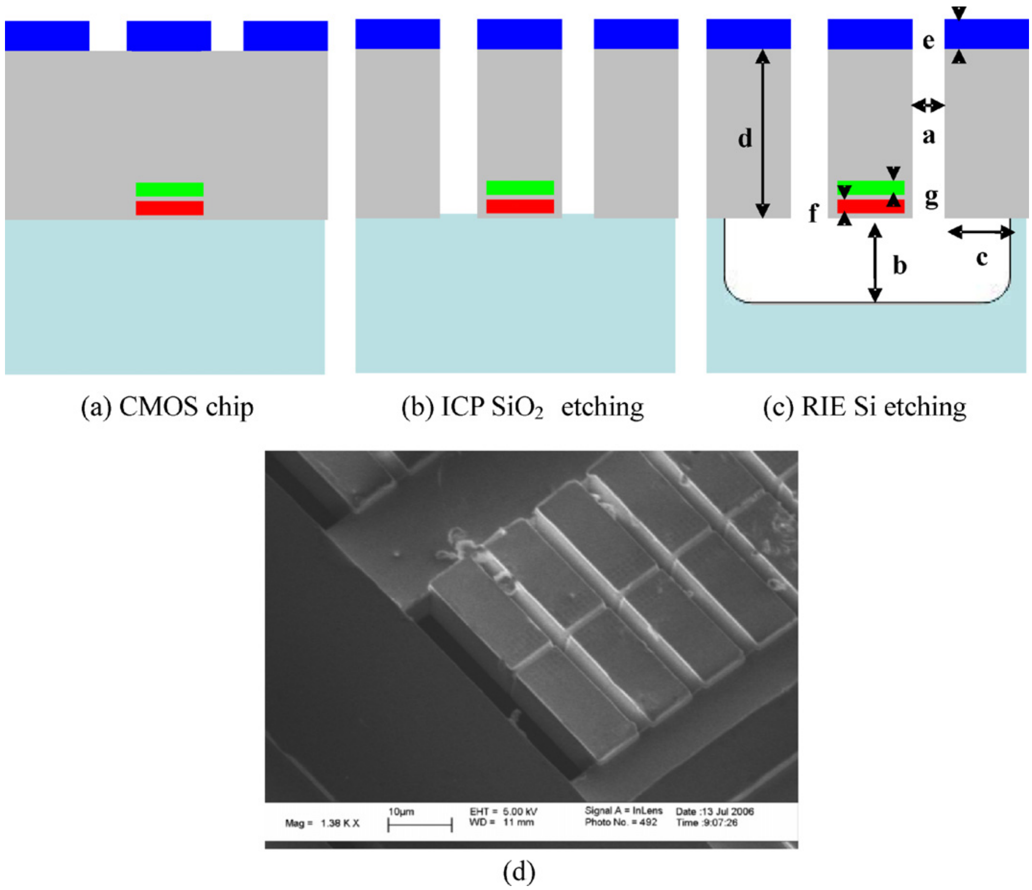

Fig. 6. (a) Thin-film depositions of the stacked thermocouple in the front- and back-end process, (b) post-CMOS process of SiO_2 vertical etching for creating the 10 μm thermal isolation cavity, and (c) Si isotropic etching where *a* is the width of etching hole (4 μm), *b* is the depth of RIE silicon etching (10 μm), *c* is the undercut of RIE silicon etching (5 μm), *d* is the depth of ICP SiO_2 etching (5 μm), *e* is the thickness of top metal mask (1 μm), *f* is the thickness of p-poly-Si (275 nm), and *g* is the thickness of n-poly-Si (180 nm), not to scale, and (d) the photomicrograph of a μTEG design (20 μm × 8 μm).

The results indicate that longer L_g requires wider W_g to achieve thermal resistance matching. For 4 μm thermoleg width, the optimal length is $L_g^* = 100\,\mu\text{m}$ and the power factor is 0.0473 μW/cm^2 K^2. Similarly at 8 μm thermoleg width, the optimal length is $L_g^* = 121\,\mu\text{m}$ and at the same power factor. Regions away from the maximums in Fig. 7(a) and (b) indicate the designs of poor thermal resistance matching, where ΔT_g is too low for thermoelectric conversion. A μTEG with excessive thermoleg length and thus high K_g allows only small thermal flow, and conversely a thermoleg with short length and low K_g can only build small temperature across the junctions. In view of the 4 μm width constraint of post-CMOS process in this work, the desired μTEG design is to have $W_g = 4\,\mu\text{m}$ at $L_g^* = 100\,\mu\text{m}$ or $W_g = 8\,\mu\text{m}$ at $L_g^* = 121\,\mu\text{m}$ for maximum power factor 0.0473 μW/cm^2 K^2. The voltage factor of the μTEGs is shown in Fig. 8(a) and (b). These characteristics imply that the desired W_g in μTEG design is first selected by considering voltage/current output requirements and then determining L_g^* for maximize power, voltage, and current. Compared with the μTEGs reported in the literature, this stacked design is shown to have the best performance and is implementable in standard CMOS process.

Table 3
Comparison with CMOS-compatible μTEGs reported in the literature.

Prior work	CMOS integrated?	Thermoelectric materials	Power factor, ϕ_p (μW/cm^2 K^2)	Voltage factor, ϕ_u (V/cm^2 K)
Glosch et al.[15]	No	Al/Si	0.091	–
Strasser et al. [13]	Yes (modified)	Poly-Si	0.0426	2.6
		Poly-SiGe	0.0352	2.2
Wang et al. [5]	No	Poly-SiGe	0.00510	0.013 (natural)0.053 (forced)
Kockmann et al. [7]	No	Al/poly-Si	0.00137	0.746
		BiTe	–	2.38
Huesgen et al. [9]	No	Al/poly-Si	0.00363	0.746
		BiTe	0.00814	2.38
Yang et al. [10]	Yes	Poly-Si	0.0417	2.417
This work	Yes	Poly-Si	0.0427	3.417

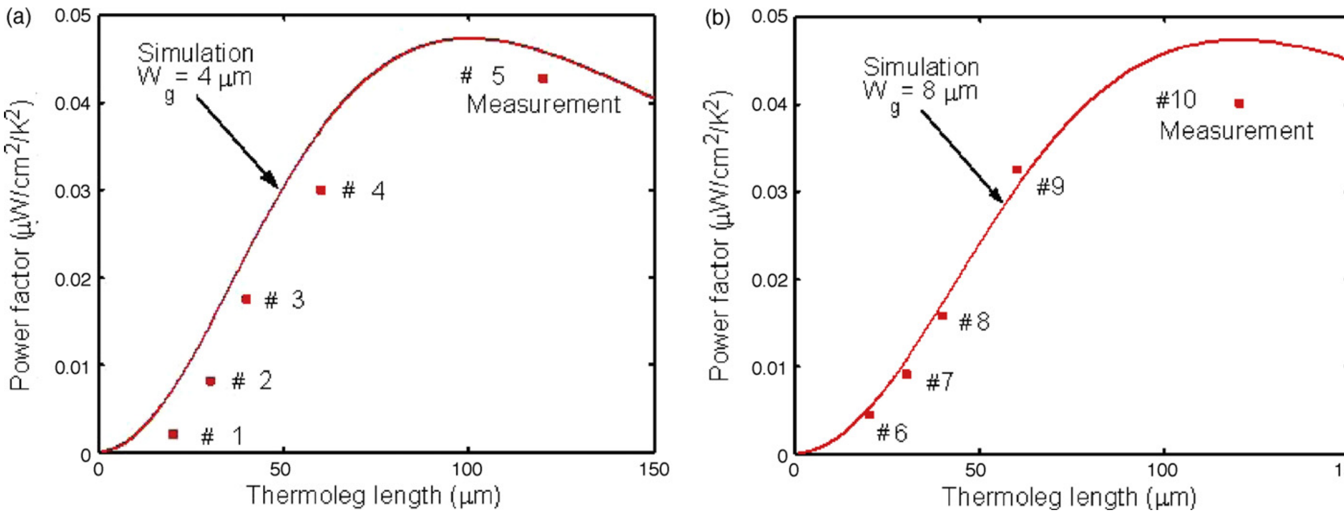

Fig. 7. (a) The measured and simulated power factor of the μTEGs in different thermoleg geometries: (a) #1–5 with $W_g = 4\,\mu m$ and (b) #6–10 with $W_g = 8\,\mu m$.

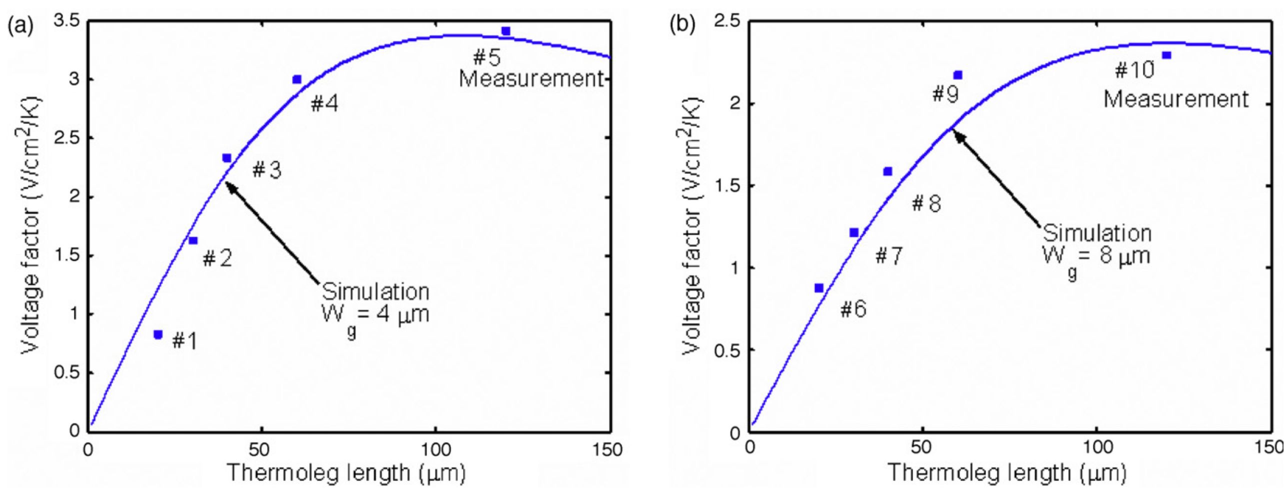

Fig. 8. (a) The measured and simulated voltage factor of the μTEGs in different thermoleg geometries: (a) #1–5 with $W_g = 4\,\mu m$ and (b) #6–10 with $W_g = 8\,\mu m$.

5. Conclusions

(1) A μTEG design based on stacked p- and n-polysilicon thermocouples is developed in this work, across which the heat input from top surface is confined passing through the thermocouple composed of two stacked and insulated thermolegs. Thermal isolation cavity design beneath the thermolegs is created to eliminate heat leakage and facilitate better thermoelectric conversion. The design is implemented by CMOS foundry process in a two-step maskless post-process. Advanced harvesters based on the stacked design by having p- and n-polysilicon layer on top of each other can maximize the area density and achieve better performance.

(2) A thermal model is applied to analyze the optimal design. Simulation results show that the maximum specific power and voltage by the optimal thermocouple $100\,\mu m \times 4\,\mu m \times 0.275/0.18\,\mu m$ (length × width × thickness for p-/n-thermolegs) are $0.0473\,\mu W/cm^2\,K^2$ and $3.952\,V/cm^2\,K$, respectively. The voltage factor is about 142% of that in co-planar design. It should be noted that the thermal model in predicting the optimal size is a 1D model, and the electrical resistance and thermal resistance in Eqs. (1a)–(1d) are assumed to be only a function of the geometric and material properties of the thermoleg. Design verification by TSMC 0.35 μm 2P4M (2-poly and 4-metal layers) standard CMOS process shows that the stacked design of a $120\,\mu m \times 4\,\mu m \times 0.275/0.18\,\mu m$ thermocouple can achieve the power factor $0.0427\,\mu W/cm^2\,K^2$ and voltage factor $3.417\,V/cm^2\,K$.

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